MAASAI MARA UNIVERSITY

REGULAR UNIVERSITY EXAMINATIONS
2019/2020 ACADEMIC YEAR

EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCIENCES

COURSE CODE: COM 2104
COURSE TITLE: COMPUTER ARCHITECTURE

DATE : 11TH DECEMBER 2019 **TIME : 2.30 -4.30 P.M**

INSTRUCTIONS:

SECTION A IS COMPULSORY ATTEMPT TWO QUESTIONS IN SECTION B

QUESTION ONE **(30 MARKS)**

a. State the basic functional units of a computer (5 marks)

b. Briefly discuss the use instruction register (IR) and program counter (PC) (4 marks)

c. Briefly describe an interrupt (2 marks)

d. Explain the concept of pipelining (2 marks)

e. Briefly discuss the following types of addressing modes (8 marks)

i. Indirect addressing mode
ii. Indexed addressing mode
iii. Autoincrement mode of addressing
iv. Autodecrement mode of addressing

f. Briefly describe RAID 1(mirroring) (3 marks)

g. Currently the most widely used technology for implementing internal memory is semiconductor technology which is classified into bipolar junction transistor and metal-oxide field effect transistor .Discuss the two technologies (6 marks)

QUESTION TWO **(20 MARKS)**

a. Briefly discuss DRAM and DDR SDRAM.(4 marks)

b. Describe the virtual memory. (2 marks)

c. Define Hit and Miss (2 marks)

d. IO devices cannot be directly be connected to the system bus, explain the reasons (4 marks)

e. Discuss the following types of Read-Only Memory (4 marks)

f. Discuss four advantages of a programmable machine (4 marks)

QUESTION THREE (20 MARKS)

a. A creative designer realizes one day that he can increase the L1 cache size of his design from 64KB to 2MB without affecting the number of cycles it takes to retrieve data from the cache and without reducing the processor frequency.

   i. What can you definitively say about this design? (2 marks)

   ii. Suppose a creative colleague of yours at FastCaches, Inc. proposed the following idea. Instead of directly using a number of bits to index into the cache, take those bits and form the index using a hash function implemented in hardware that randomizes the index.
   What type of cache misses can this idea potentially reduce? (2 marks)

   iii. The hash function randomizes the mapping of each cache block to a set so that set conflicts (e.g. due to unlucky data alignment or aliasing) are less likely.
   What is a disadvantage of the idea other than the additional hardware cost of the hash function? (2 marks)

b. Exceptions need to be handled when detected by the processor (and known to be non-speculative) whereas interrupts can be handled when convenient.

   i. Why does an exception need to be handled when it is detected? In no more than 20 words, please. (2 marks)

   ii. What does it mean to handle an interrupt \when it is convenient"? (2 marks)

   iii. Why can many interrupts be handled \when it is convenient"? (2 marks)

c. A program spends 75% of its time doing multiply instructions.

   i. If the multiplier is sped up by 3x, how much faster does the application run? (Report your answer as “the program is X times faster.”)
   (2 marks)

   ii. What is the limit on the maximum speedup if the multiplier in question above was infinitely fast? (Report your answer as “the program would be X times faster.”) (2 marks)

d. DMA is wore for large transfers than interrupts due to the overhead of setting up the transfer. True or false. Explain (2 marks)

e. Explain how the data is organized in the disk (2 marks)

QUESTION FOUR (20 MARKS)

a. Briefly discuss the use of cache memory(2 marks)

b. In the designing of buses basic parameters are considered. The parameters that serve to classify and differentiate buses are bus type, method of arbitration, timing, bus width and data transfer types. Discuss these parameters (10 marks)

c. Schemes for timing of data transfers over a bus can be classified into synchronous and asynchronous, discuss the advantages and disadvantages of asynchronous bus (4 marks)

d. Discuss the factors considered in designing an I/O subsystem (4 marks)

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